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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,507	09/26/2003	Derek Knee	10016660-3	3741

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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,507	KNEE, DEREK	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,12,14,19,21 and 26-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,12,14,19,21 and 26-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some* c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9-26-2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Receipt is acknowledged of the Pre-Amendment filed September 26, 2003.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 12, 14, 19, 21, and 26-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Menon et al. (US PAT No. 6,218,858) in view of Aude et al. (US PAT No. 6,486,821).

Regarding claim 1, Figs. 5 and 7 of Menon et al. discloses a CMOS circuit (Fig. 5 is implemented in 154 of Fig. 7; col. 6, line 61 - col. 7, line 11) comprising a differential logic circuit (the same NMOS 88, 90 are differentially coupled in Fig. 5; col. 5, lines 64-65) having a plurality of logic inputs (IN and REF in Fig. 5; REF can be substituted with the complementary of IN; col. 6, lines 23-25), and a current source (98 in Fig. 5) supplying bias current to the differential logic circuit (col. 6, lines 5-7), but does not disclose the differential logic circuit fabricated of thin oxide transistors and the current source fabricated using at least one thick oxide transistor by a fabrication process (thick oxide transistors and thin oxide transistors by a fabrication process is the "product-by-process" limitation. Regarding the "product-by-process" claims, it should be noted that a "product-by-

process" claim is directed to the product per se, no matter how such a product was made. It has been well established by the Courts that it is the Patentability of the final product per se which must be determined in a "product-by-process" claim, and not the Patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claim in "product-by-process" form or not.

See *In re Hirao*, 190 USPQ 15 at 17 (footnote 3); *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessman*, 180 USPQ 324; *In re Avery*, 186 USPQ 161, *In re Marosi et al.*, 218 USPQ 289; and in particular *In re Thorpe*, 227 USPQ 964. It should be noted that the applicant has the burden of proof in such cases, as the above case law makes clear.).

However, Fig. 1 of Aude et al. discloses the differential logic circuit (111, 112) fabricated of thin oxide transistors (col. 4, lines 64-66) and the current source (115) fabricated using at least one thick oxide transistor (col. 4, line 66 - col. 5, line 2) for the purpose of providing an differential amplifier that operates from higher voltage supply for the thick oxide transistors while the thin oxide transistors operate from lower voltage supply and has the improved open-loop gain and bandwidth.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to construct the differential logic circuit and the current source of Menon et al. with thin oxide transistors and thick transistors of Aude et al. respectively because it would provide capabilities of integrating two different operating power supply voltages.

Regarding claim 2, Fig. 5 and 7 of Menon et al. modified by Aude et al. discloses the CMOS circuit of claim 1, and Menon et al. further discloses where the current source has a control input (the gate of 98) that can determine how much current is available to source to the differential logic circuit (the control signal, NBIAS, determines the amount of current flowing through 88 and 90; col. 6, lines col. 6, lines 5-7).

Regarding claim 3, Fig. 5 and 7 of Menon et al. modified by Aude et al. discloses the CMOS circuit of claim 2 (Fig. 7 is the top level where Fig. 5 is implemented as LPECL/LVDS INPUT circuit 154; col. 6, line 61 - col. 7, line 11), and Menon et al. further discloses an adaptive bias control (programming bits stored in internal memories in the FPGA in Fig. 7; col. 7, lines 57-62) that provides a control signal (NBIAS) at the control input of the current source (98) to increase the bias current available to the differential logic circuit (NBIAS control the bias current; col. 6, lines 5-7).

Regarding claim 12, Figs. 5 and 7 of Menon et al. discloses a CMOS circuit (Fig. 5 is implemented in 154 of Fig. 7; col. 6, line 61 - col. 7, line 11) comprising a differential logic circuit (the same NMOS 88, 90 are differentially coupled in Fig. 5; col. 5, lines 64-65) having a plurality of logic inputs (IN and REF in Fig. 5; REF can be substituted with the complementary of IN; col. 6, lines 23-25), and a current source (98 in Fig. 5) supplying bias current to the

differential logic circuit (col. 6, lines 5-7), the current source having a control input (gate terminal of 98 in Fig. 5) that can determine how much current is available to source to the differential logic circuit (NBIAS signal applied at the gate terminal of 98 in Fig. 5 determines the amount of current flowing through 88 and 90; col. 6, lines col. 6, lines 5-7), an adaptive bias control (programming bits stored in internal memories in the FPGA in Fig. 7; col. 7, lines 57-62) that provides a control signal (NBIAS) at the control input of the current source (98 in Fig. 5) to selectively control the bias current available to the differential logic circuit (NBIAS control the bias current; col. 6, lines 5-7), but does not disclose the differential logic circuit fabricated of thin oxide transistors and the current source fabricated using at least one thick oxide transistor by a fabrication process (thick oxide transistors and thin oxide transistors by a fabrication process is the "product-by-process" limitation. Regarding the "product-by-process" claims, it should be noted that a "product-by-process" claim is directed to the product per se, no matter how such a product was made. It has been well established by the Courts that it is the Patentability of the final product per se which must be determined in a "product-by-process" claim, and not the Patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claim in "product-by-process" form or not.

See *In re Hirao*, 190 USPQ 15 at 17 (footnote 3); *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessman*, 180 USPQ 324; *In re Avery*, 186 USPQ 161, *In re Marosi et al.*, 218 USPQ 289; and in particular *In re Thorpe*, 227

USPQ 964. It should be noted that the applicant has the burden of proof in such cases, as the above case law makes clear.).

However, Fig. 1 of Aude et al. discloses the differential logic circuit (111, 112) fabricated of thin oxide transistors (col. 4, lines 64-66) and the current source (115) fabricated using at least one thick oxide transistor (col. 4, line 66 - col. 5, line 2) for the purpose of providing an differential amplifier that operates from higher voltage supply for the thick oxide transistors while the thin oxide transistors operate from lower voltage supply and has the improved open-loop gain and bandwidth.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to construct the differential logic circuit and the current source of Menon et al. with thin oxide transistors and thick transistors of Aude et al. respectively because it would have provide capabilities of integrating two different operating power supply voltages.

Regarding claim 14, Figs. 5 and 7 of Menon et al. modified by Aude et al. discloses the CMOS circuit according to claim 12, and Menon et al. further discloses a bias load circuit (102 and 104 in Fig. 5) loading the differential logic circuit (col. 6, lines 7-11).

Regarding claim 19, Figs. 5 and 7 of Menon et al. discloses a CMOS circuit (Fig. 5 is implemented in 154 of Fig. 7; col. 6, line 61 - col. 7, line 11) comprising a differential logic circuit (88, 90 are differentially coupled in Fig. 5;

col. 5, lines 64-65) having a plurality of logic inputs (IN and REF in Fig. 5; REF can be substituted with the complementary of IN; col. 6, lines 23-25), the differential logic circuit comprising a pair of the same NMOS devices (88, 90) configured as a differential inverter (complementary IN is inverted at the output node 118; and IN is inverted at the node between 102 and 88) and a current source (98 in Fig. 5) supplying bias current to the differential logic circuit (col. 6, lines 5-7), the current source comprising a transistor (98 in Fig. 5) receiving a supply voltage (96 in Fig. 5) at a drain thereof, the current source having a control input (NBIAS in Fig. 5) at a gate (100 in Fig. 5) thereof that can determine how much current is available to source to the differential logic circuit (NBIAS signal applied at the gate terminal of 98 in Fig. 5 determines the amount of current flowing through 88 and 90; col. 6, lines col. 6, lines 5-7), an adaptive bias control (programming bits stored in internal memories in the FPGA in Fig. 7; col. 7, lines 57-62) that provides a control signal (NBIAS) at the control input of the current source (98 in Fig. 5) to selectively control the bias current available to the differential logic circuit (NBIAS control the bias current; col. 6, lines 5-7), but does not disclose the differential logic circuit fabricated of thin oxide transistors comprising a pair of matched thin oxide transistor and the current source fabricated using at least one thick oxide transistor by a fabrication process (thick oxide transistors and thin oxide transistors by a fabrication process is the "product-by-process" limitation. Regarding the "product-by-process" claims, it should be noted that a "product-by-process" claim is directed to the product per se, no matter how such a product was made. It has been well established by the

Courts that it is the Patentability of the final product per se which must be determined in a "product-by-process" claim, and not the Patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claim in "product-by-process" form or not.

See *In re Hirao*, 190 USPQ 15 at 17 (footnote 3); *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessman*, 180 USPQ 324; *In re Avery*, 186 USPQ 161, *In re Marosi et al.*, 218 USPQ 289; and in particular *In re Thorpe*, 227 USPQ 964. It should be noted that the applicant has the burden of proof in such cases, as the above case law makes clear.).

However, Fig. 1 of Aude et al. discloses the differential logic circuit (111, 112) fabricated of thin oxide transistors (col. 4, lines 64-66) being a pair of matched thin oxide transistor (pair of 111 and 112 are made with the same +1.8 volt process) and the current source (115) fabricated using at least one thick oxide transistor (col. 4, line 66 - col. 5, line 2) for the purpose of providing an differential amplifier that operates from higher voltage supply for the thick oxide transistors while the thin oxide transistors operate from lower voltage supply and has the improved open-loop gain and bandwidth.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to construct the differential logic circuit and the current source of Menon et al. with matched thin oxide transistors and thick transistors of Aude et al. respectively because it would provide capabilities of integrating two different operating power supply voltages.

Regarding claim 21, Figs. 5 and 7 of Menon et al. modified by Aude et al. discloses the CMOS circuit according to claim 19, and Menon et al. further discloses a bias load circuit (102 and 104 in Fig. 5) loading the differential logic circuit (col. 6, lines 7-11).

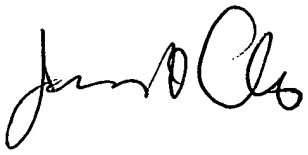
Regarding claims 26-31, Figs. 5 and 7 of Menon et al. modified by Aude et al. discloses the CMOS circuit according to claims 1, 12 and 19 where thin oxide transistors of the differential logic circuit fabricated by the fabrication process are each characterized as having a higher switching speed and a higher transconductance gm than the at least one thick oxide transistor of the current source fabricated by the fabrication process and the at least one thick oxide transistor fabricated by the fabrication process is operable to operate in a higher voltage condition than can the plurality of thin oxide transistors fabricated by the fabrication process and is further characterized as being larger and slower in operation than the plurality of thin oxide transistors (it is inherent that the transconductance of a transistor is inversely proportion to the size of oxide thickness, that is, the thinner the oxide thickness means greater transconductance. The greater conductance inherently means the smaller resistance, and the less resistance inherently functions faster speed).

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



James H. Cho
Primary Examiner
Art Unit 2819

July 26, 2004